V PLUS U	A Trusted Institute of DPP
SUBJECT : TOPIC:	TIME: DATE:
1. Given below are symbols for some logic gates	(a) XOR gate(b) NOR gate(c) AND gate(d) OR gate
(1) (1) (2) (2) (3) (4) The XOR gate and NOR gate respectively are $(a) 1 and 2$ $(b) 2 and 3$ $(c) 3 and 4$ $(d) 1 and 4$	 5. The truth table shown in figure is for A 0 0 1 1 B 0 1 0 1 Y 1 0 0 1 (a) XOR (b) AND (c) XNOR (d) OR
2. Given below are four logic gate symbol (figure). Thos for OR, NOR and NAND are respectively $A \leftarrow y = B \leftarrow y = A \leftarrow y$	 6. The logic behind 'NOR' gate is that it gives (a) High output when both the inputs are low (b) Low output when both the inputs are low (c) High output when both the inputs are high (d) None of these
$A \xrightarrow{y} A \xrightarrow{y} $	 7. A logic gate is an electronic circuit which (a) Makes logic decisions (b) Allows electrons flow only in one direction (c) Works binary algebra (d) Alternates between 0 and 1 values
3. The combination of 'NAND' gates shown here under (figure) are equivalent to $A \bullet \bigcirc $	8. A gate has the following truth table $\begin{array}{cccccccccccccccccccccccccccccccccccc$
 (a) An OR gate and an AND gate respectively (b) An AND gate and a NOT gate respectively (c) An AND gate and an OR gate respectively (d) An OR gate and a NOT gate respectively. 	9. Which of the following gates will have an output of 1 (a) $\begin{pmatrix} 1 \\ 0 \end{pmatrix}$ (b) $\begin{pmatrix} 0 \\ 1 \end{pmatrix}$ (c) $\begin{pmatrix} 0 \\ 1 \end{pmatrix}$ (d) $\begin{pmatrix} 0 \\ 0 \end{pmatrix}$ (d) $\begin{pmatrix} 0 \\ 0 \end{pmatrix}$
 A truth table is given below. Which of the following ha this type of truth table A 0 1 0 1 B 0 0 1 1 	10. Which represents NAND gate
y 1 0 0 0 SCO 16-17 HUDA MARKET URBAN	(a) (b) NESTATE JIND HARYANA 9053013302

